Fermilab
Particle Physics/Electrical Engineering Department

The CMS Hadron Calorimeter Front-End Module

Introduction

The CMS Hadron Calorimeter Front-End Module, pictured in figure 1, is used to digitize the analog signals of over 10,000 detector channels. As seen in figure 2, the FE module resides in a Readout Box[1](RBX) located on the detector. A backplane[2], located within the RBX, provides the FE module with power, clocks and a slow controls communication path.

Figure 3 is a block diagram representation of the FE module. As can be seen, the architechture of the module is fairly straightforward. Each module can read out six channels of data. Six QIE[3] ASICs are used to collect charge from detector channels and to digitize it. That digitized data, 5 bits of mantissa, 2 exponent bits and 2 capacitor ID tags are then passed over to three Channel Control ASICs[4] (CCA). Finally, the CCA's feed the data into a high speed serial link, utilizing the Gigabit Optical Link[5] (GOL) ASIC. The data is then sent to data concentrator crates for further processing.

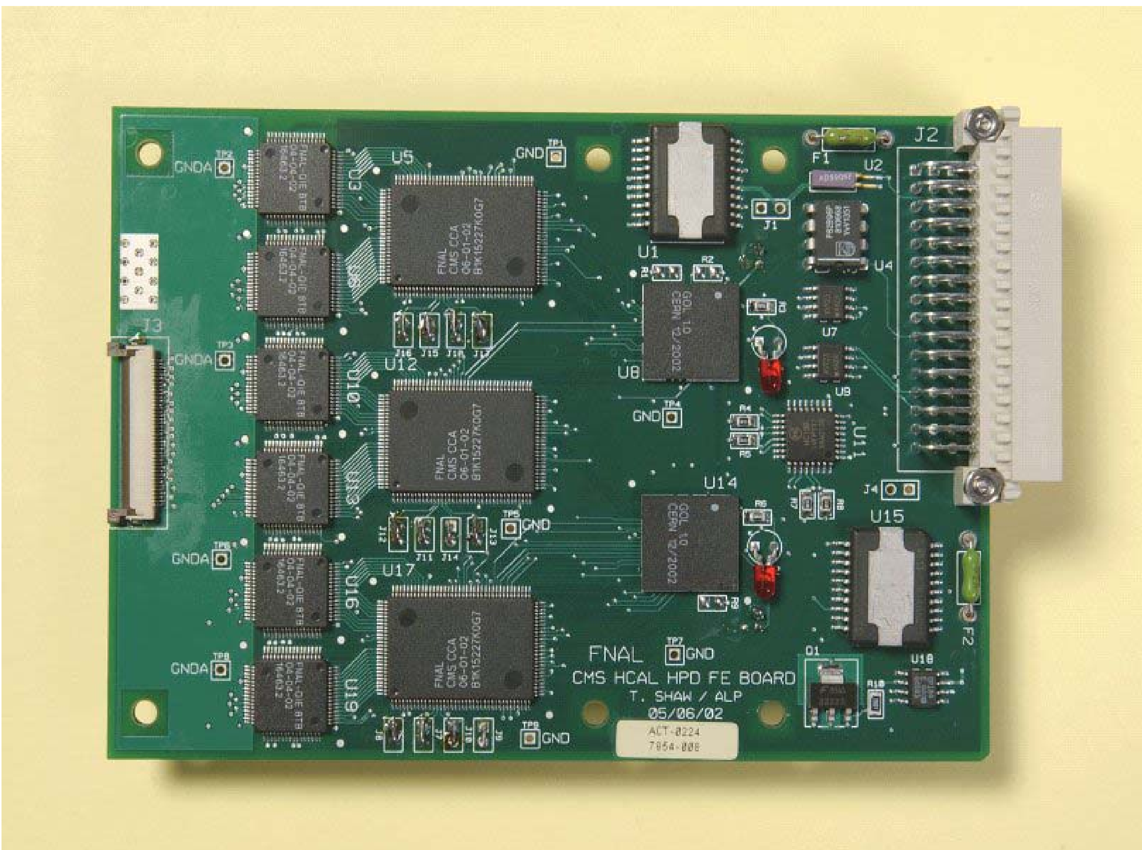

Figure 1. Photograph of the Testbeam 2002 Front End Module

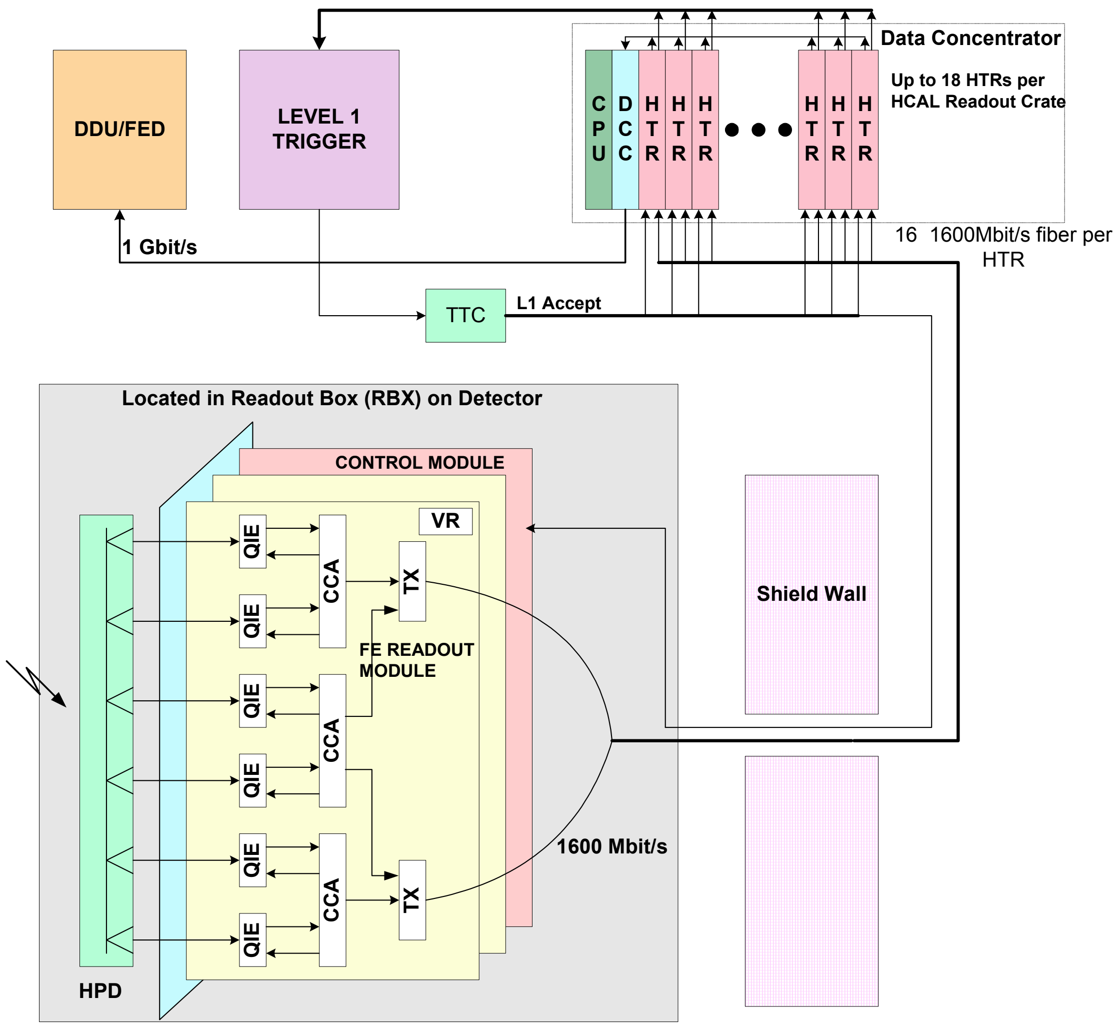

Figure 2. Readout System Overview

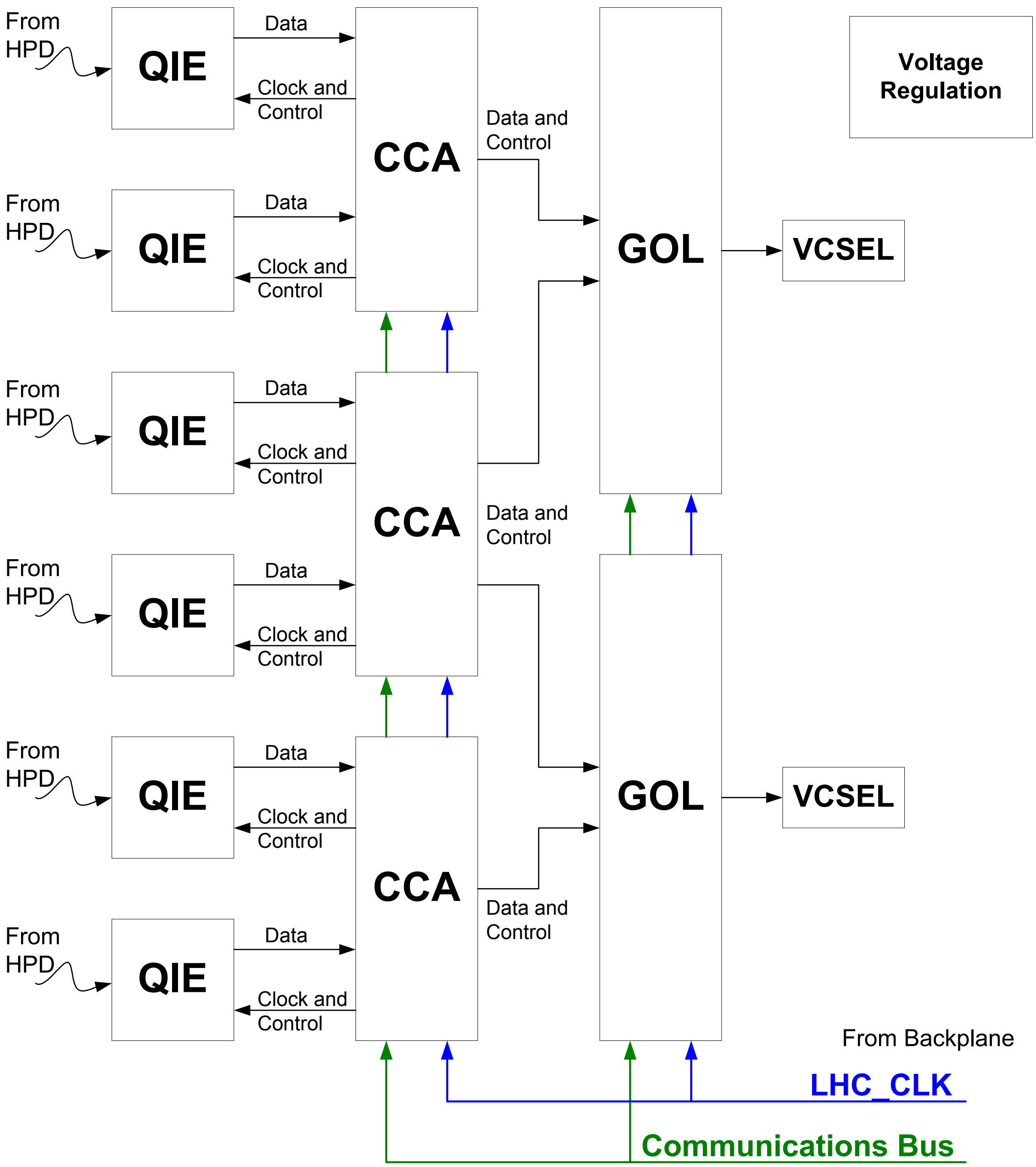

Figure 3. Front End Module Block Diagram

Input Section

The input section of the FE module consists of 6 QIEs, each handling a single channel. The source of the input signals is a Hybrid Photo Diode[6] (HPD) which receives inputs from scintillating fibers fed through an Optical Decoder Unit[7] (ODU), see figure 4.

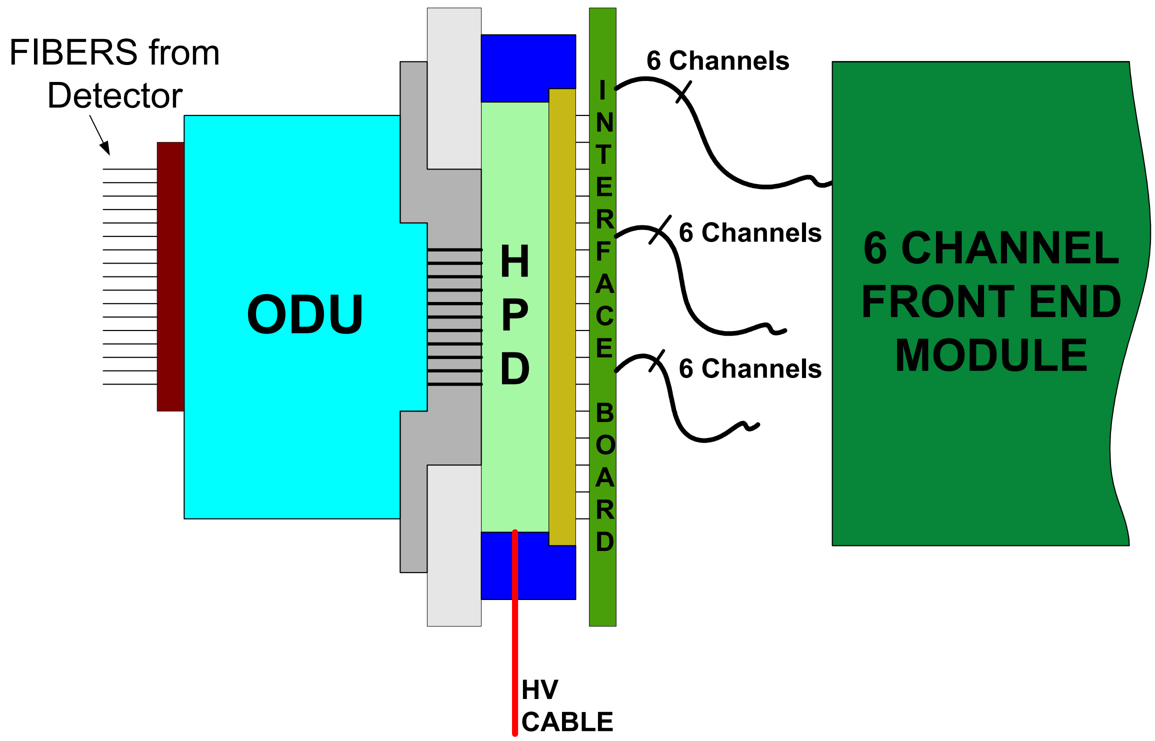

Figure 4. Detector Signals Input Path

The QIE signals are brought into the FE Module on a 26 conductor flat flex cable. The pinout on the cable is shown in Table 1.

FE Module Pin #	Signal
1	Gnd
2	Ref_signal_0
3	Gnd
4	Input_signal_0
5	Gnd
6	Ref_signal_1
7	Gnd
8	Input_signal_1
9	Gnd
10	Ref_signal_2
11	Gnd
12	Input_signal_2
13	Gnd
14	Ref_signal_3
15	Gnd
16	Input_signal_3
17	Gnd
18	Ref_signal_4
19	Gnd
20	Input_signal_4
21	Gnd
22	Ref_signal_5
23	Gnd
24	Input_signal_5
25	Gnd
26	Gnd

Table 1. FE Module Input Connector Pinout

QIE/CCA Interface

The QIE and CCA ASICs work in tandem on the FE Module. The QIE receives all of the control signals it requires from the CCA, and all its generated data is sent to the CCA. It is assumed that the reader is familiar with the QIE and CCA specifications, if not, please refer to documents listed in the Reference section. Figure 5 illustrates the connections found between the QIE and the CCA. Please note that two QIEs are served by a single CCA.

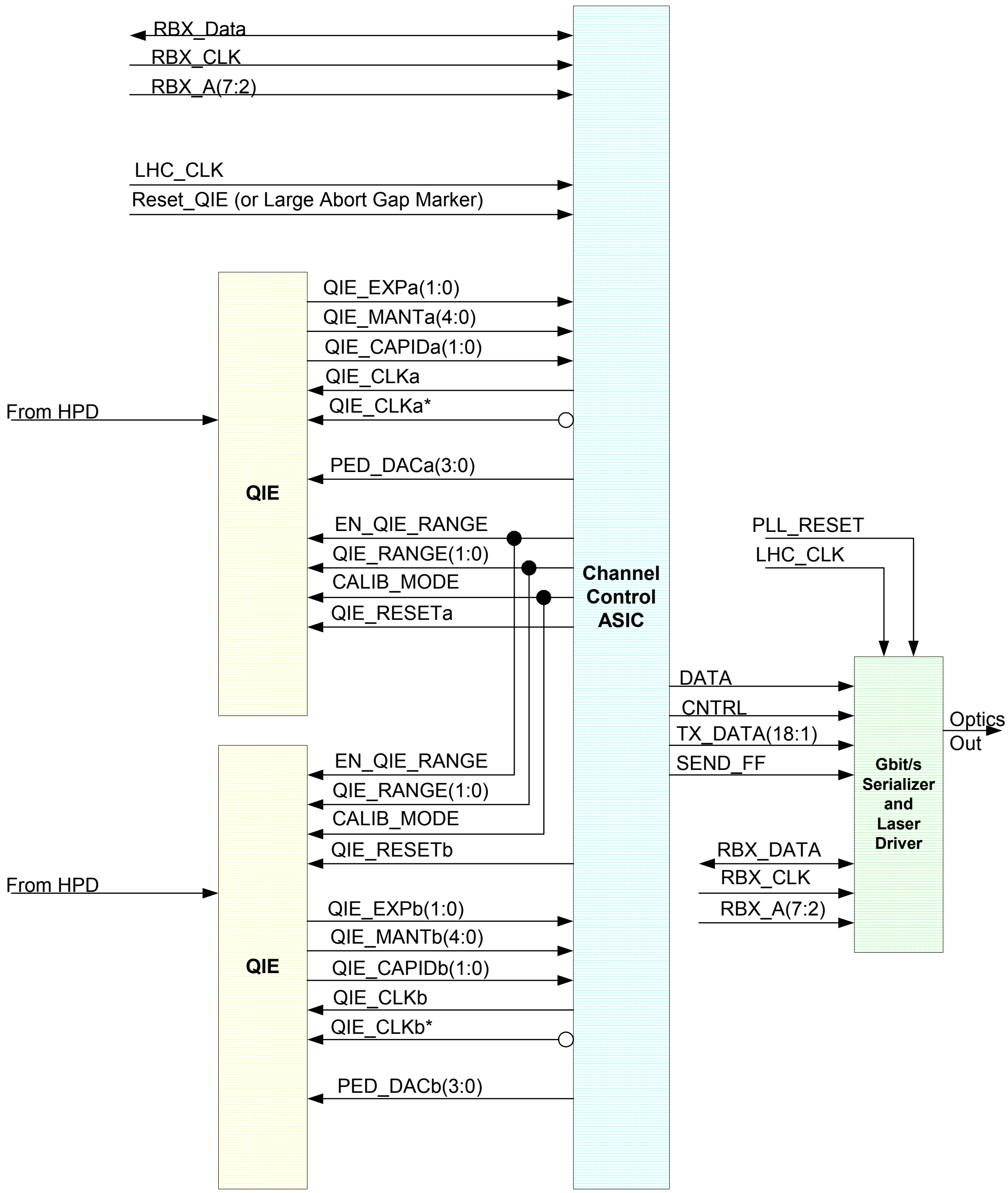

Figure 5. QIE and CCA Interface

Output Section

The data output from the CCA is sent to the GOL serializer. The GOL is being used in 32 bit 8B/10B mode. The laser driver output of the GOL is used to drive a VCSEL. Data on the optical fiber is being sent at 1600 Mbps.

As can be seen in Figure 3, data from 3 CCAs is sent to two GOLs. Thus; each optical fiber driven by a GOL contains the data of 3 detector channels.

The format of the data is shown in Figure 6.

	D(31:30)	D(29:25)	D(24)	D(23:22)	D(21:17)	D(16)	D(15:14)	D(13:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	QIE 0 Exp (1:0)	QIE 0 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 1 Exp (1:0)	QIE 1 Mant (4:0)	"0"	QIE 2 Exp (1:0)	QIE 2 Mant (4:0)	QIE 0 CapID(1:0)	QIE 1 CapID(1:0)	QIE 2 CapID(1:0)	Control Flag=0	Data Flag=1	"1"
Optical Cable 2	QIE 4 Exp (1:0)	QIE 4 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 5 Exp (1:0)	QIE 5 Mant (4:0)	"0"	QIE 3 Exp (1:0)	QIE 3 Mant (4:0)	QIE 4 CapID(1:0)	QIE 5 CapID(1:0)	QIE 3 CapID(1:0)	Control Flag=0	Data Flag=1	"1"

FE DATA FORMAT

	D(31:25)	D(24)	D(23:21)	D(20)	D(19)	D(18:17)	D(16)	D(15:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	Bunch Count A (0:6)	QIE_Reset (abort gap marker?)	Bunch Count A (9:11)	Bunch Count Error A	CapID Error A	"XX"	"0"	Bunch Count B (0:6)	Bunch Count A (7:8)	"XX"	Bunch Count B (7:8)	Control Flag=1	Data Flag=0	"1"

	D(31:25)	D(24)	D(23:21)	D(20)	D(19)	D(18:17)	D(16)	D(15:13)	D(12)	D(11)	D(10:9)	D(8:7)	D(6:3)	D(2)	D(1)	D(0)
Optical Cable 2	Bunch Count C (0:6)	QIE_Reset (abort gap marker?)	Bunch Count C (9:11)	Bunch Count Error C	CapID Error C	"XX"	"0"	Bunch Count B (9:11)	Bunch Count Error B	CapID Error B	"XX"	Bunch Count C (7:8)	"XXXX"	Control Flag=1	Data Flag=0	"1"

FE Orbit Message - Normal message

	D(31:25)	D(24)	D(23:17)	D(16)	D(15:9)	D(8)	D(7)	D(6:5)	D(4)	D(3)	D(2)	D(1)	D(0)
Optical Cable 1	Test Pattern "N" A(0:6)	QIE_Reset (abort gap marker?)	Test Pattern "N+1" A(1:7)	"0"	Test Pattern "N" B(0:6)	Test Pattern "N+1" A(0)	Test Pattern "N" A(7)	"XX"	Test Pattern "N+1" B(0)	Test Pattern "N" B(7)	Control Flag=0	Data Flag=1	"1"

	D(31:25)	D(24)	D(23:17)	D(16)	D(15:9)	D(8)	D(7)	D(6:2)	D(2)	D(1)	D(0)
Optical Cable 2	Test Pattern "N" C(0:6)	QIE_Reset (abort gap marker?)	Test Pattern "N+1" C(7:1)	"0"	Test Pattern "N+1" B(7:1)	Test Pattern "N+1" A(0)	Test Pattern "N" A(7)	"XXXX"	Control Flag=0	Data Flag=1	"1"

FE Orbit Message - Test Pattern message

23-Nov-03

Figure 6. Fiber Optic Cable Data Format

Control Section

Control of FE Module is accomplished through a backplane signals. The backplane pinout is shown in Table 2.

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V2	V2	V2
7	GND	GND	GND
8	MCLK+	GND	SERCLK+
9	MCLK-	GND	SERCLK-
10		GND	SER_DAT
11	TEMP	GND	RESET_PLL+
12		GND	RESET_PLL-
13	GEO_ADDR(0)	GND	RESET+
14	GEO_ADDR(1)	GND	RESET-
15	Reset_QIE+	GND	PWR_RESET
16	Reset_QIE-	GND	PWR_Trip

Table 2. FE Module Backplane Signals

The backplane pins have the following functions on the FE Module:

V1 (power)
Input voltage of 6.5V, which is regulated on board to 5.0V. This supplies power to the QIEs and temperature transducer.

V2 (power)
Input voltage of 4.5V, which is regulated on board to 3.3V and 2.5V. This supplies power to all parts other than QIEs and the temperature transducer.

MCLK+/- (input)
Differential LVPECL signal which supplies the 40MHz LHC clock signal.

TEMP (output)
Single ended line which provides a temperature measurement from the module. This is the output of a temperature transducer.

GEO_ADDR(1:0) (input)

Geographic address pin on the backplane. The two pins provide address encoding for slot position within a group of three modules, see Table 3. These pins have weak pull-ups on the FE modules, so that grounded pins have an address of logic "0", and floating pins have a logic level of "1".

Slot #	**GEO_ADDR(1)**	**GEO_ADDR(0)**
0	GND	GND
1	GND	float
2	float	GND

Table 3. Geographical Slot Encoding

Reset_QIE+/- (input, active high)

Differential LVPECL signal which generates a QIE reset and an Orbit Message. The Orbit Message takes the place of QIE data on the Optical data link for 70 clock cycles. The "Reset_QIE" signal is required to reset the QIEs upon power-up and should be used whenever it is believed that the QIEs may be malfunctioning due to an SEU. At least one "Reset_QIE" signal must be sent across the backplane before the FE module will be in a working state.

The "Reset_QIE" signal was originally intended to be sent to the Front end at the beginning of the large abort gap during each cycle of the beam. The CCA ASIC must see this signal at a fixed point in the Orbit in order for its error checking and programmable pulse signals to function correctly. However, the Front end will work fine and issue a steady uninterrupted stream of data if it sees this signal only once upon power up.

RESET+/- (input, active low)

Differential LVPECL signal which supplies the reset signal to the CCA. This reset signal must be sent at or after power up in order to ensure the proper operation of the CCA. In addition, this reset will reset all CCA register values to the default value.

RESET_PLL+/- (input, active low)

Differential LVPECL signal which supplies the reset signal to the GOL and the CCA's Delay Lock Loop. This reset signal must be sent at or after power up in order to ensure the proper operation of the GOL and CCA. In addition, this reset will reset the CCA delay lock loop, without effecting the CCA register values.

PWR_RESET (input, active high)

Single-ended LVTTL signal used to reset the power circuit of the FE Module. This must be applied after power is initially applied to the circuit, prior to any other operations, as well as whenever an over current trip of the power circuit has occurred.

PWR_Trip (output, active high)
A wired-or line which will signal that a FE module has had an over current trip.

Communication Bus Signals – I^2C like protocol

SERCLK+/- (input)
Differential LVPECL signal which supplies the clock signal for the 2-wire communication bus used to communicate with the CCA and GOL. This is effectively the "SCL" signal of the I^2C-like communication interface built into those ASICs.

SERDAT (bi-directional, open drain)
This is a bi-directional line which is effectively the "SDA" signal of the I^2C-like communication interface built into those ASICs.

Serial Communication Bus Address Space

Each FE module has three CCAs and two GOLs, all of which have downloadable registers which control their functions. Both the CCA and the GOL interface to the serial bus in a similar manner; they both use an Address_Pointer Register and a Data Register to access any of their internal registers.

Read and write operations follow the I^2C protocol. When reading the Data Register, the contents of the register pointed to by the Address_Pointer Register is transferred. When writing to the Data Register, the data is actually tranferred to the register being addressed by the Address_Pointer Register.

Like I^2C, a seven bit address field is used by the communication bus to address the chips. An address map of this register space is given in Table 4 below.

Register	**Address(7:6)**	**Address(5:2) (bin)**	**Address(1)**
CCA – Channels 0,1			
Address_Ptr	Geo_Addr(1:0)	0000	0
Data	Geo_Addr(1:0)	0000	1
CCA – Channels 2,3			
Address_Ptr	Geo_Addr(1:0)	0001	0
Data	Geo_Addr(1:0)	0001	1
CCA – Channels 4,5			
Address_Ptr	Geo_Addr(1:0)	0010	0
Data	Geo_Addr(1:0)	0010	1
GOL – Channels 0,1,2			
Address_Ptr	Geo_Addr(1:0)	0100	0
Data	Geo_Addr(1:0)	0100	1
GOL – Channels 0,1,2			

Address_Ptr	Geo_Addr(1:0)	0101	0
Data	Geo_Addr(1:0)	0101	1

Table 4. FE Module I^2C Address space

Example: To write value 0x77 (77 hex) to the Pedestal DAC Register (internal CCA address of 0x03) of the CCA controlling Channels 0 and 1 and which is located in slot 1, the user would send an I^2C write of value 0x03 to address "0100000". This sets the Address_Ptr Register of the CCA to point to its internal Pedestal DAC Register. Next the user would follow with an I^2C write of 0x77 to address "0100001". The second operation would transfer the value 0x77 into the Pedestal DAC Register of the CCA controlling channels 0 and 1 of the card in slot 1.

Detailed information on the internal CCA and GOL registers can be found in their specifications, listed in the reference section of this document.

Power Section

The FE board receives two unregulated voltages from the backplane. One voltage, V1 or 6.5V, is regulated down to 5.0V by an ST Microelectronics LHC4913[8] rad hard voltage regulator. This voltage is used by the QIEs and the temperature transducer.

The second voltage, V2 or 4.5V, is regulated down to 3.3 V and 2.5V. These voltages are used to power the digital portions of the FE module.

Voltage	Power
V1 (6.5V)	5 Watts
V2 (4.5V)	4 Watts

Table 5. Power Table

The power circuit has been designed to turn off the voltage regulators whenever an over current situation has been sensed. An SCR switch holds keeps the regulator turned off until it senses the PWR_RESET signal from the backplane.

References

1) RBX - TBD
2) T. Shaw, "Specification for the CMS HCAL Readout Box Backplane", Sept. 19, 2001.
3) T. Zimmerman, et. al., "Specification for Production CMS QIE ASIC (QIE8)", Revised September 27, 2002.
4) T. Shaw, et. al., "Specification for the CMS Hadron Calorimeter Front End Readout Module Channel Control ASIC", Revised March 8, 2002.
5) P. Moreira, "GOL Reference Manual", May 2002.
6) P. Cushman, "Problems and Solutions in high-rate multi-channel Hybrid Photodiode design: The CMS Experience", IEEE NSS 2001 Conference, November 2001.
7) ODU – TBD
8) LHC4913 3 Amp Positive Low Drop Voltage Regulator with Inhibit, ST Microelectronincs, July 2000.